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Design And Implementation Of Efficient Multiplier Architectures

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ABSTRACT - The main purpose of the project is to improve the speed of the digital circuits like multiplier since adder and multiplier are one of the key hardware components in high performance systems such as microprocessors, digital signal processors and FIR filters etc. Hence we always try for efficient multiplier architecture to increase the efficiency and performance of a system. The efficiency of the multiplier can be improved by applying Vedic sutras. This 'Vedic Mathematics' is the name given to the ancient system of mathematics or, to be precise, a unique mathematical problem can done with the help of arithmetic, algebra, geometry or trigonometry can be solved. Multiplication plays an important role in the processors. It is one of the basic arithmetic operations and it requires more hardware resources and processing time than the other arithmetic operations. Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Karatsubha – Ofman algorithm. In this project high speed, low power 8x8, 16x16 and 32x32 multipliers are designed and it is implemented in FIR adder Xilinx ISE 8.1i.

Index terms - Multiply and Accumulate(MAC), Computation- Intensive Arithmetic Functions (CIAF), Digital Signal Processing (DSP), Fast Fourier Transform (FFT), Complementary Metal Oxide Semioconductor (CMOS), Arithmetic and Logic Unit (ALU), Binary Coded Decimal (BCD), Discrete Cosine Transform (DCT)

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate (MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier.

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level

the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption. The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective.

Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. The computation time taken by the array multiplier is comparatively less because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array. Booth multiplication is another important multiplication algorithm. Large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. Multiplication of two n-bit operands using a radix-4 booth recording multiplier requires approximately n / (2m) clock cycles to generate the least significant half of the final product, where m is the number of Booth recorder adder stages. Thus, a large propagation delay is associated with this case. Due to the importance of digital multipliers in DSP, it has always been an active area of research and a number of interesting multiplication algorithms have been reported in the literature.

In this, Urdhva tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This is shown to be very similar to the popular array multiplier architecture. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier structures. Nikhilam Sutra is then discussed and is shown to be much more efficient in the multiplication of large numbers as it reduces the multiplication of two large numbers to that of two smaller ones. The multiplication algorithm is then illustrated to show its computational efficiency by taking an example of reducing a 4X4-bit multiplication to a single 2X2-bit multiplication operation. This work presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics .The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics.

Multiplication is the most important arithmetic operation in signal processing applications and inside the Processor. As speed is always a major requirement in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematics was reconstructed from the ancient Indian scriptures

(Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time.

Multiplication is an important arithmetic operations which is used frequently in hardware level in digital filtering where currently implementations applied in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms and also they are required many in numbers than the other hardware component, so there is a need of high speed multiplier to increase the speed of the multiplier. Still, multiplication time of the hardware multiplier is the important factor in determining the instruction cycle time of a DSP chip. The demand for high speed DSP has been increasing as a result of expanding computer and signal processing applications. Arithmetic operations like multiplication are important to achieve the desired performance in many real-time digital signal and image processing applications. The development of fast multiplier circuits has been a subject of interest from two decades. Reducing the time delay and power consumption are very essential requirements for any digital applications as they mostly works on battery. This analysis gives different Vedic multiplier architectures with karatsuba algorithm.

Multipliers based on Vedic Multiplication are one of the fast and low power multipliers. Minimizing power consumption for digital systems involves optimization at all levels of the design and in Vedic multiplication this is achieved due to less steps to solve the multiplication than the traditional multiplication. This optimization includes the technology used to implement the digital circuits requirements are circuit style, topology, and the architecture for implementing the circuits and at the highest level the algorithms. In Digital designs multipliers are the most commonly used components. They are fast, mostly used and efficient components that are utilized to implement many operations. Depending upon the algorithms of the components, there are so many types of multipliers available. Particular multiplier architecture is selected based on the desired application. In many DSP algorithms, the multipliers are in the critical delay path and ultimately determine the overall algorithm performance. The speed of multiplication operation is of great importance in DSP as well as in general processor.

A. Vedic Mathematics

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful. The word "Vedic" is derived from the word **"Veda"** which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like

arithmetic, algebra, geometry etc[15]. These Sutras along with their brief meanings are enlisted below alphabetically.

B. Vedic multiplication Sutras

The 16 Vedic multiplication Sutras along with their brief meanings are enlisted below alphabetically.

1. Ekadhikina Purvena – In this method we have to find one more than the previous sequence.
2. Ekanyunena Purvena – In this method we have to find one less than the previous sequence.
3. (Anurupye) Shunyamanyat – If one multiplicand is in the ratio, the other is zero.
4. Chalana-Kalanabyham – multiplication is found by the Differences and Similarities between multiplier and multiplicand.
5. Gunakasamuchyah – in these method factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – in this method product of the sum is equal to the sum of the product.
7. Paraavartya Yojayet – multiplication is found by the Transpose and adjusts.
8. Puranapuranabyham – multiplication is found by the completion or noncompletion.
9. Nikhilam Navatashcaramam Dashatah – – in this method product of all from 9 and last from
10. Sankalana- vyavakalanabhyam – multiplication is found by the addition and by subtraction.

11. Sopaantyadvayamantyam – multiplication is found by the ultimate and twice the penultimate.

12. Urdhva-tiryagbhyam – multiplication is found by the vertically and crosswise.

13. Shesanyankena Charamena – multiplication is found by the remainders by the last digit.

14. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.

15. Vyashtisamanstih – multiplication is found by the Part and Whole.

16. Yaavadunam – multiplication is found by whatever the extent of its deficiency.

These sutras can be used in various trigonometric as well as the geometric problems in mathematics effectively. These Sutras were reconstructed from ancient Vedic texts. Many Sub-sutras were also discovered till now which gives its distinctive advantages, which are not discussed here. The advantage of Vedic mathematics lies in the fact that it reduces the otherwise complex calculations in conventional mathematics to a very simple one. This is so because the Vedic sutras are claimed to be based on the natural principles on which the human brain works. This is a very remarkable field and presents some effective algorithms which can be applied to various branches of engineering such as computing, digital signal processing and digital image processing. The multiplier architectures can be broadly classified into three categories. First one is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations where the drawback is the relatively larger chip area utilization. Third one is serial- parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

C. Brief description of Sutras

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charamena – The remainders by the last digit.

12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century. Many Sub-sutras were also discovered at the same time, which are not discussed here. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. The multiplier architecture can be generally classified into three categories. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second is parallel multiplier (array and tree) which carries out high speed mathematical operations. But the drawback is the relatively larger chip area consumption. Third is serial-parallel multiplier which serves as a good trade-off between the times consuming serial multiplier and the area consuming parallel multipliers.

II DESIGN OF VEDIC MULTIPLIER

The Vedic multiplication hardware model basic structure is shown in figure 2.1.The below figure 2.2 show the line diagram of Urdhva tiryakbhyam.This is the another method of Urdhva tiryakbhyam to perform multiplication. This method is mostly use in most of the implementation of processors.

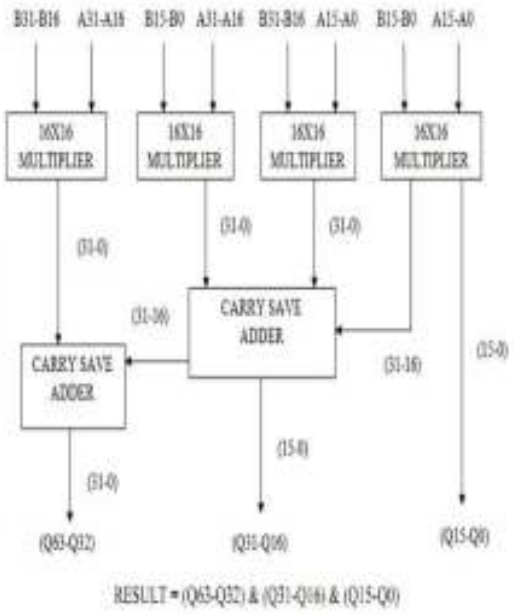

Figure 2.1 Vedic Multiplier hardware model

A. Karatsuba – Ofman Algorithm

Multipliers are the basic and essential building blocks of many high performance systems. Multiplication is frequently used operation which is currently implemented in many processors. In today's market there is a huge demand for high speed multipliers, since these are the slowest elements in the systems. The speed of the multiplier decides the speed of the system; hence the speed of the multiplier has to be improved. The performance of the system depends on the multiplier's speed which is optimized by the proposed multiplier. Vedic mathematics is the ancient system of mathematics. The word 'Vedic' is derived from the word 'Veda', which means store-house of all knowledge.. Karatsuba Ofman is the fast multiplication algorithm which helps to increase the speed of the multiplier. Pipelining has long been known as efficient technique for optimising the computational time. Significant speed-up in computational time is increased by the application of pipelining. Pipelining comes as a rescue for speeding-up the clock frequency. With

the aid of Pipelining and with Karatsuba-Ofman algorithm, will double the speed of the proposed KOPM multiplier.

Karatsuba-Ofman's algorithm is one of the fastest methods to multiply long integers. This multiplication algorithm multiplies every digit of a multiplicand by every digit of the multiplier and adds the result to the partial product. It has O(n 2) complexity, where n is the operand size (number of digits).Karatsuba-Ofman algorithm has O(n 1.585) complexity and thus it multiplies large numbers faster. Let A and B be two n-digit numbers in radix z where n is even. Divide these two numbers into two parts and can be written as,

$A = A_H Z^{n/2} + A_L$

$B = B_H Z^{n/2} + B_L$

where Z=2 for binary number system, A_L and A_H are the lower digits (first n/2) and higher digits(last n/2) of number A respectively. Similarly B_L and B_L are the lower digits (first n/2) and higher digits(last n/2) of number B. The product P can be calculated as,

$P = A \cdot B = (A_H Z^{n/2} + A_L) \cdot (B_H Z^{n/2} + B_L)$

$P = A_L B_L + (A_L B_H + A_H B_L) Z^{n/2} + (A_H B_H) Z^n$ ..... (1)

Illustration: Let A = 1001 (9) and B = 0010 (2) Now, A = (10)2 2 + (01) B = (00)2 2 + (10) P = (01)(01) + [(10)(00)] 2 4 + [(01)(00) + (10)(00)] 22 = 0010 + 00000000 + [0000 + 0100] 2 2 = 0010 + 00000000 + 010000 = 00010010 (18)

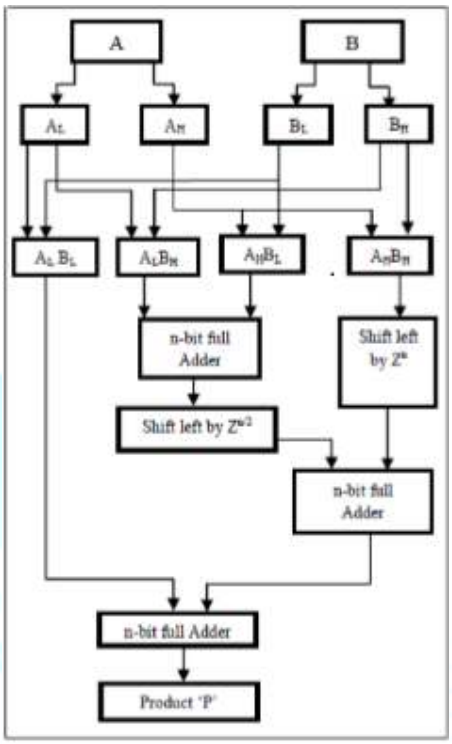

Figure 2.1 Karatsuba – Ofman Algorithm

Thus product P can be calculated by solving equation (1) with four partial products: $A_L B_L$, $A_L B_H$, $A_H B_L$ and $A_H B_H$. The block diagram of Karatsuba-Ofman Algorithm is shown in figure 1 which requires three adders.

B. Urdhava Line Diagram

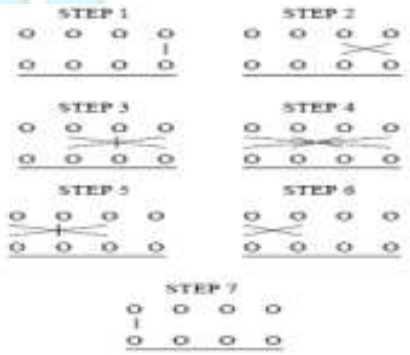

Figure 2.2 Urdhava Line diagram

Here we can see that urdhava method done multiplication in single shift which increase the

speed of processors. This algorithm is not efficient for large number because of lot of propagation delay is involved. In order to deal with this propagation delay problem Nikhilam Sutra is present which is efficient method for large number multiplications.

C. Urdhva Tiryakbhyam In 2x2 Vedic Multiplier

The most prominently used sutras of the 16 mention sutras are Urdhva tiryakbhyam Sutra which literally means "Vertically and crosswise". To demonstrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional method will require 16 multiplications and 15 additions. Multiplication using Urdhva tiryakbhyam Sutra is shown in Figure 2.3. The numbers to be multiplied are written on two consecutive sides as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a Multiplicand. Where, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are separated into two halves by the crosswise lines. Each digit of the multiplier is then autonomously multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits on a crosswise dotted line are added to the subsequent carry.

The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

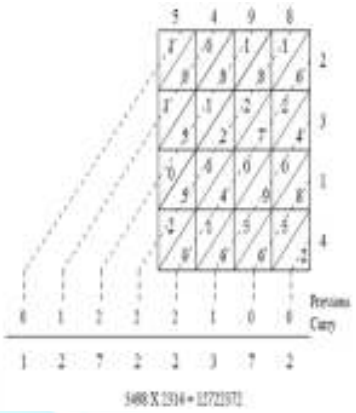

Figure 2.3 Multiplication by Urdhva tiryakbhyam Sutra

D. Mathematical Background Of "Urdhva-Tiryakbyham" Sutra

Assume that X and Y are two numbers, to be multiplied. Mathematically X and Y can be represented in the equation (1) and (2) as:

$$A = \sum_{i=0}^{N-1} Ai10^{i} \quad \text{----------} \quad (1)$$

$$B = \sum_{j=0}^{N-1} Bj10^{j} \quad \text{----------} \quad (2)$$

Assume that, their product is equal to Z. Then Z can be represented as:

$$Z = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} Ai \quad Bj10^{i+j} \quad \text{----------} \quad (3)$$

Where (Ai , Bj € (0,1,2,.....,9) and 'N' may ne any number.

From the above equation (3), it can observed that each digit is multiplied consecutively and shifted towards the proper positions for partial product generation. Finally the partial products are added with the previous carry to produce the final results.

The design starts first with Multiplier design that is 2x2 bit multiplier as shown in figure 3.4.

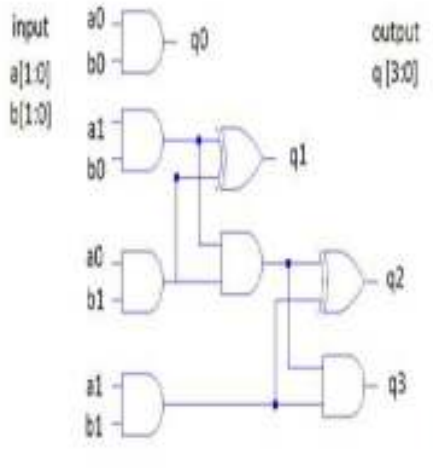

Figure 2.4 Hardware Realization of 2x2 blocks

Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products. To scale the multiplier further, Karatsuba – Ofman algorithm can be employed. Karatsuba-Ofman algorithm is considered as one of the fastest ways to multiply long integers. It is based on the divide and conquers strategy.

E. 4x4 Vedic Multiplier

Integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation.

The multiplier architecture is based on Urdhva Tiryagbhyam (vertical and cross-wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra is shown in Figure 2.5.

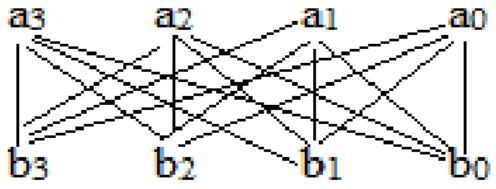

Figure 2.5 Illustration of Urdhva Tiryagbhyam sutra

The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra, whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. Consider two 4-bit binary numbers a3a2a1a0 and b3b2b1b0. The partial products (P7P6P5P4P3P2P1P0) generated are given by the following equations:

i. P0= a0b0

ii. P1= a0b1 + a1b0

iii. P2 = a0b2 + a1b1 + a2b0+ P1

iv. P3= a0b3 + a1b2 + a2b1 + a3b0+ P2

v. P4 = a1b3 + a2b2 + a3b1 + P3

vi. P5 = a1b2 + a2b1 + P4

vii. P6 = a3b3 + P5

viii. P7 = carry of P6

F. Urdhva Tiryakbhyam In 4x4 Vedic Multiplier

An The "Urdhva Tiryagbhyam" Sutra is a general multiplication formula applicable to all cases of multiplication such as binary, hex, decimal and octal. The Sanskrit word "Urdhva" means "Vertically" and "Tiryagbhyam" means "crosswise". Figure 3.6 shows an example of Urdhva Tiryagbhyam. **Algorithm:** Multiplication of 101 by 110 1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the answer. 2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together. 3. Multiply the LSB digit of bottom number with the MSB digit of the top one, LSB digit of top number with the MSB digit of bottom and then multiply the second bit of both, and then add them all together. 4. This step is similar to the second step, just move one place to the left. We

will multiply the second digit of one number by the MSB of the other number. Finally, simply multiply the LSB of both numbers together to get the final product.

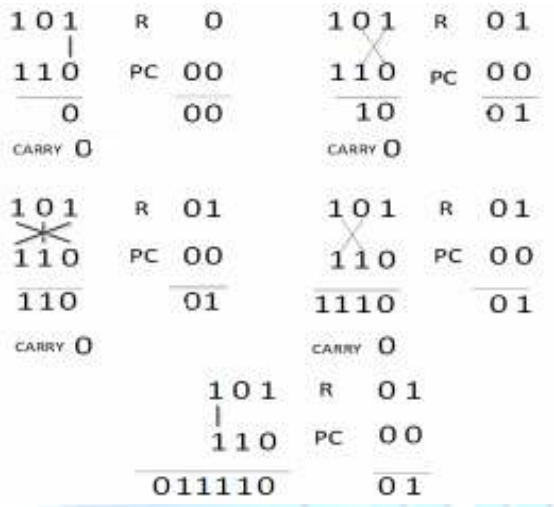

Figure 2.6 Urdhva Tiryagbhyam Procedure for Multiplication

The partial products are generated parallel and concurrent additions of the partial products are done using this algorithm. Because of this the speed of the multiplier is increased considerably when compared to other techniques.

G. Existing 4x4 Vedic Multiplier

This (figure 3.7) is the existing 4x4 Vedic multiplier, which is having four 2x2 Vedic multiplier and three 4 bit ripple carry adder.

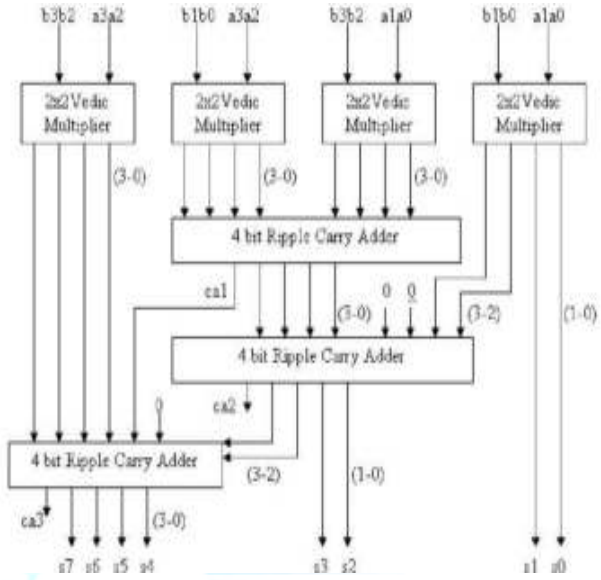

Figure 2.7 Existing 4x4 Vedic Multiplier

H. 4-Bit Adder

The 4-bit adder performs the function of 4-bit addition that gives two bits of sum and one carry as output. Its block diagram contains one full adder (FA) and two half adders (HF) is given in Figure 2.8 .

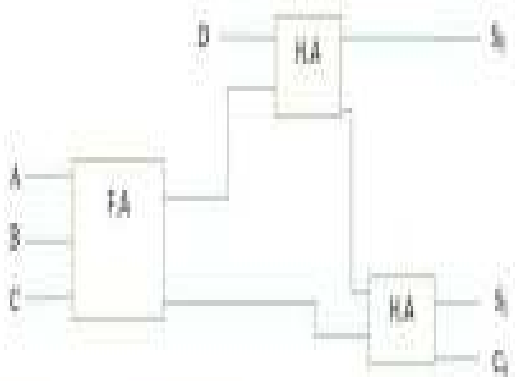

Figure 2.8 4-bit adder

Here, A, B, C, D are four inputs. S0 and S1 are LSB and MSB of Sum outputs respectively and Sum is the sum of four inputs. C0 is the carry bit. To reduce the delay, a 4X4 multiplier is implemented using half adder, full adder and the 4-bit adder as shown in Figure 2.9.

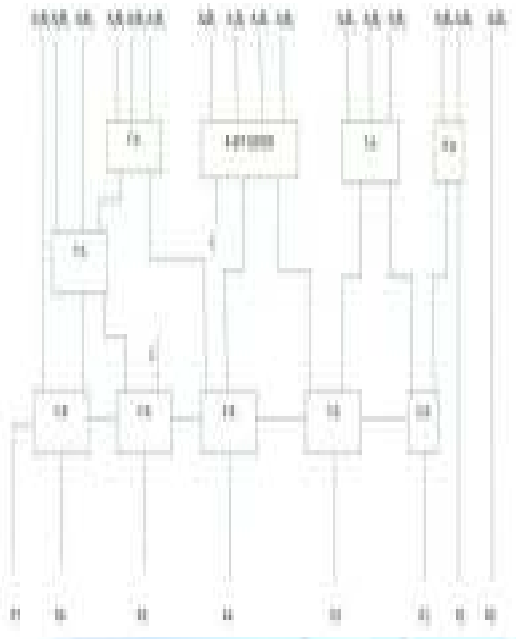

Figure 2.9 4x4 multiplier using 4 - bit adder

I. CARRY SAVE ADDER

A Carry save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits. The block diagram of carry save adder is shown in figure 2.10 and the example is shown in the figure 2.11

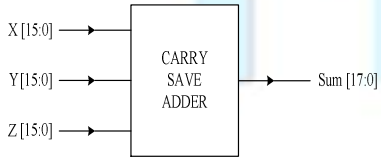

Figure 2.10 Block Diagram of Carry save adder

The drawback is that we know the result of the addition at once. We still do not know whether theresult of the addition is larger or smallerthan the given number (for instance we do not know whether the number is positive or negative)

This latter is the drawback when using carry save adders to implement modular multiplication.

Example for carry save addition

X:	1 0 0 1 1		X:	1 0 0 1 1	
Y:	+ 1 1 0 0 1		Y:	+ 1 1 0 0 1	
Z:	+ 0 1 0 1 1		Z:	+ 0 1 0 1 1	
C:	1 1 0 1 1		S:	0 0 0 0 1	

X:	1 0 0 1 1
Y:	+ 1 1 0 0 1
Z:	+ 0 1 0 1 1
S:	0 0 0 0 1
C:	1 1 0 1 1
Sum:	1 1 0 1 1 1

Figure 2.11 Example of Carry save adder

J.SERIAL ADDER

The serial adder is a digital circuit that performs binary addition bit by bit. The serial full adder has three single bit inputs for the numbers to be added and the carry - in. There are two single bit outputs for the sum and carry- out. The carry – in signal is the previously calculated carry – out signal. The addition is performed by adding each bit, lowest to highest, one per clock cycle. The block diagram of serial adder is shown in the figure 2.12. This serial adder is used in vedic multiplier in order to reduce the area and power consumption.

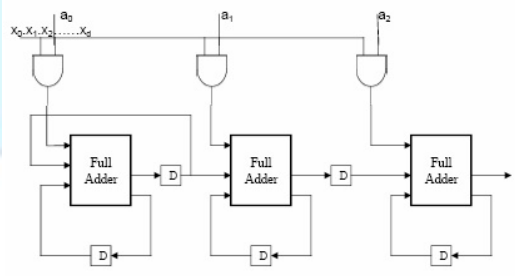

Figure 2.12 Block diagram of serial adder

III RESULTS AND DISCUSSION

The proposed 32x32 vedic multiplier is designed and simulated using Modelsim and Xilinx

ISE 8.1i. The simulation result for 32x32 Vedic multiplier is given below

The layout generated in Modelsim for the 32x32 Vedic multiplier is shown in the Figure 3.1

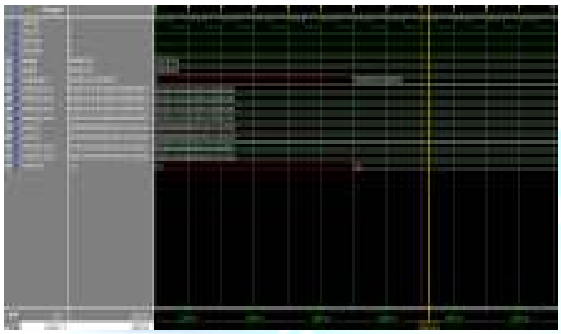

Figure 3.1 The simulation result of 32x32 Vedic multiplier

The simulation result for the area utilisation of 32x32 Vedic multiplier is shown in Figure 3.2

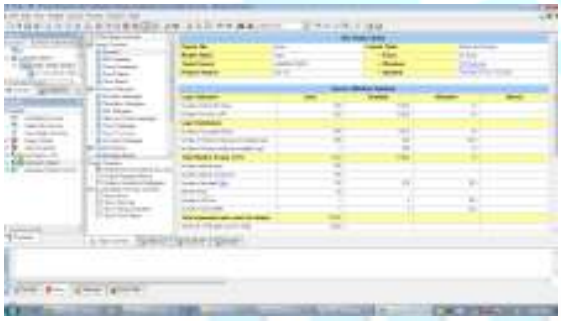

Figure 3.2 Area Utilisation of 32x32 Vedic Multiplier

The rea utilisation of 32x32 Vedic multiplier with serial adder is 26.874

The simulation result for the delay of 32x32 Vedic multiplier is shown in Figure 3.3

Figure 3.3 Timing Diagram of 32x32 Vedic multiplier

The delay of 32x32 Vedic multiplier with serial adder is 4.964ns

The simulation result for power consumption is shown in Figure 3.4

Figure 3.4 The Power consumption of 32x32 Vedic multiplier

The Power consumption of 32x32 Vedic multiplier is 433mW.

The 8x8, 16x16 and 32x32 Vedic multiplier is designed. The Vedic Multiplier is compared with the existing multiplier architecture in terms of area utilisation, delay and power consumption. The results obtained are tabulated in Table 3.1. From the Table 3.1, it is evident that there is a reduction in both area and power consumption. The area for the existing multiplier architecture is 26.874. The power consumption for the existing multiplier is 12.028. Thus, it is clear that the Vedic Multiplier is more efficient then the existing one. The Vedic Multiplier can be used to develop a high speed complex number multiplier with reduced area and power consumption.

Table 3.1 Comparison between existing multiplier architectures and Vedic multipliers

	Existing Vedic Multiplier with CSA	**Proposed Vedic Multiplier with Serial adder**
Area utilisation	26.874	12.028
Delay (ns)	4.964	8.253
Power Consumption (mW) [4]	463	433

IV CONCLUSION

This project presents a novel way of realizing a high speed multiplier using Karatsuba – Ofman Algorithm. The designs of 8x8, 16x16 and 32x32 bits Vedic multiplier have been implemented using Modelsim and Xilinx ISE 8.1i. The design is based on Vedic method of multiplication using serial adder. The Vedic multipliers gives a total delay of 8.253 ns. The power consumption of the Vedic multiplier is 433mW which is very less when compared to the existing Multiplier architectures. The area utilisation is 12.028 which is very less when compared to the existing multiplier rchitectures. It is therefore seen that the Vedic multipliers are much more faster than the conventional multipliers. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased. Karatsuba – Ofman algorithm reduce the area utilisation and power consumption and hardware requirements for multiplication of numbers. The high speed multiplier algorithm exhibits improved efficiency in terms of speed. Our design is more preferable over all other designs. It is also implemented in FIR filter design.

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